



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,501	09/22/2004	Glenn G. Daves	FIS920040002US1	5500
29505 7590 10/18/2007 LAW OFFICE OF DELIO & PETERSON, LLC. 121 WHITNEY AVENUE NEW HAVEN, CT 06510			EXAMINER ABOAGYE, MICHAEL	
			ART UNIT 1793	PAPER NUMBER
			MAIL DATE 10/18/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,501	DAVES ET AL.	
	Examiner	Art Unit	
	Michael Aboagye	1793	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 October 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 and 13-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 13-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 2, 4, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over White (US Patent No. 5,535,526) in view of Yan et al. (US Patent No. 6,841,888).

White discloses an electronic module and a method of making said module, the method comprising: attaching a chip (402, figure 4) to a substrate (404, figure 4) using a first solder interconnection array (406, figure 4); attaching an organic board (416, figure 6, and column 1, lines 6-15) to said substrate using a second solder interconnection array (412, figure 4) such that a space is defined between said board and said substrate having a gap height ranging from about 300 microns to about 900 microns (note white in figure 4, shows two bond pads (each, 5 mil thickness or diameter) to a solder ball (5 mil diameter), see column 1, lines 25-32), therefore the gap height between the substrate and the board is about equal to the stack height of the bond pads and the solder ball (15mils which is equivalent to 345.5 microns, and this meets the gap limitation recited in claim1); said second solder interconnection array residing entirely within said space

Art Unit: 1793

(see, figure 4); and providing an underfill material within said space after said board has been attached to said substrate but prior to applying compressive forces to said electronic module (408, figure 4 and column 7, lines 24-46), Note the applicant in his own admission as per figure 1 and paragraph 8, that it is common practice to apply compressive force to the assembly after attaching the board to the substrate. White providing a mechanical support structure comprising at least one rigid metallic ball within said space (column 5, lines 42-47) and providing a mechanical support structure comprising a frame (916, figure 9) within said space (White see, column 8, lines 25-28).

White does not expressly teaches an underfill with filler and also the filler particle size and composition of said filler. White also teaches dual melt solder interconnect (White, column 2, lines 35-52 and column 5, lines 48-60).

Yan et al. teaches an underfill for use in an opto-electronic device comprising filler particles of particle size of about 250 microns or 500 microns (column 7, lines 10-15, and column 11, lines 40-46), present in amount of about 60% (Yan et al. column 7, lines 5-15, and column 16, lines 39-45), density of about 1.32g/cc and viscosity greater than 5,000 cP (column 12, lines 1-5) and glass transition temperature greater than 120 degrees (Yan et al. column 1, lines 37-44); wherein said filler material present in the underfill is used to vary the thermal coefficient of the underfill and thereby match the thermal coefficient of the substrate or the board and to prevent damaging of the electronic module (Yan et al. column 1, line 62-column 2, line 20).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to provide a filler in the underfill used in the process of

Art Unit: 1793

White as taught by Yan et al. since, filler material present in the underfill can be used to vary the thermal coefficient of the underfill to match the thermal coefficient of the substrate or the board and thereby preventing thermal damage to the electronic module (Yan et al., column 1, line 62-column 2, line 20).

3. Claims 1, 2,4,19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over White (US Patent No. 5,535,526) in view of Yan et al. (US Patent No. 6,841,888) as applied to claim 1 above and further in view of Matsuda (US Patent No. 6,697,261).

White and Yan et al. do not expressly teach a mechanical support bracket in the assembly.

Matsuda teaches a process for manufacturing an electronic module using solder interconnect, comprising a mechanical standoff member (75, figure 26), (interpreted by the examiner as a bracket) to keep a predetermined space between the substrate (11, figure 26) and a component (12, figure 260, so that the solder bumps (13(a, b)) can be prevented from excessive squashing under the application of compressive force (Matsuda column 12, lines 37-61).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to provide a standoff member or a bracket in the combined invention of White and Yan et al. as taught by Matsuda to prevent the solder bumps from being excessively squashed under the application of compressive force (Matsuda column 12, lines 37-61).

Art Unit: 1793

4. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over White (US Patent No. 5,535,526) in view of Yan et al. (US Patent No. 6,841,888) as applied to claims 1 and 19 above and further in view of Morganelli et al. (US Patent No. 7,047,633).

White. and Yan et al. do not expressly teach an underfill material partially encapsulating said second solder interconnection array at discrete locations

However, Morganelli et al., teaches an electronic an a method of forming said package having a solder interconnect and applying underfill to partially encapsulate fraction of the height of the solder bump in the space or gap between the interconnect, thereby allowing a space for volatile compounds to escape from the package during a reflow process (Morganelli et al., column1, lines 10-30, and column 8, lines 15-20).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to use partial underfill in the combined process of White. and Yan et al. as taught by Morganelli et al. to allow a space for volatile compounds to escape from the package during a reflow process (Morganelli et al., column1, lines 10-30, and column 8, lines 15-20).

5. Claims 5,7-10, 13 and 14, are rejected under 35 U.S.C. 103(a) as being unpatentable over White (US Patent No. 5,535,526) in view of Yan et al. (US Patent No. 6,841,888) and Morganelli et al. (US Patent No. 7,047,633).

Art Unit: 1793

White discloses an electronic module and a method of making said module, the method comprising: attaching a chip (402, figure 4) to a substrate (404, figure 4) using a first solder interconnection array (406, figure 4); attaching an organic board (416, figure 6, and column 1, lines 6-15) to said substrate using a second solder interconnection array (412, figure 4) such that a space is defined between said board and said substrate having a gap height ranging from about 300 microns to about 900 microns (note white in figure 4, shows two bond pads (each, 5 mil thickness or diameter) to a solder ball (5 mil diameter), see column 1, lines 25-32), therefore the gap height between the substrate and the board is about equal to the stack height of the bond pads and the solder ball (15mils which is equivalent to 345.5 microns, and this meets the gap limitation recited in claim1); said second solder interconnection array residing entirely within said space (see, figure 4); and providing an underfill material within said space after said board has been attached to said substrate but prior to applying compressive forces to said electronic module (408, figure 4 and column 7, lines 24-46), Note the applicant in his own admission as per figure 1 and paragraph 8, that it is common practice to apply compressive force to the assembly after attaching the board to the substrate. White providing a mechanical support structure comprising at least one rigid metallic ball within said space (column 5, lines 42-47) and providing a mechanical support structure comprising a frame (916, figure 9) within said space (White see, column 8, lines 25-28). White teaches a ceramic substrate and an organic board (column 5, lines 30-35) and that since the CTE value is a material property, Said a ceramic substrate and an organic board similarly a ceramic substrate has a CTE below Tg of about 18 ppm/°C to about 21

Art Unit: 1793

ppm/°C and said organic substrate has a CTE below T_g of about 12 ppm/°C to about 25 ppm/°C.

White does not expressly teaches an underfill with filler and also the filler particle size and composition of said filler. White also teaches dual melt solder interconnect (White, column 2, lines 35-52 and column 5, lines 48-60).

Yan et al. teaches an underfill for use in an opto-electronic device comprising filler particles of particle size of about 250 microns or 500 microns (column 7, lines 10-15, and column 11, lines 40-46), present in amount of about 60% (Yan et al. column 7, lines 5-15, and column 16, lines 39-45), density of about 1.32g/cc and viscosity greater than 5,000 cP (column 12, lines 1-5) and glass transition temperature greater than 120 degrees (Yan et al. column 1, lines 37-44); wherein said filler material present in the underfill is used to vary the thermal coefficient of the underfill and thereby match the thermal coefficient of the substrate or the board and to prevent damaging of the electronic module (Yan et al. column 1, line 62-column 2, line 20). Yan et al. also teaches

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to provide a filler in the underfill used in the process of White as taught by Yan et al. since, filler material present in the underfill can be used to vary the thermal coefficient of the underfill to match the thermal coefficient of the substrate or the board and thereby preventing thermal damage to the electronic module (Yan et al., column 1, line 62-column 2, line 20).

White. and Yan et al. do not expressly teach an underfill material partially encapsulating said second solder interconnection array at discrete locations.

However, Morganelli et al., teaches a method of forming and electronic module using solder interconnect and applying underfill to partially encapsulate a fraction of the space or gap between the solder interconnect, thereby allowing a space for volatile compounds to escape from the package during a reflow process (Morganelli et al., column1, lines 10-30, and column 8, lines 15-20).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to use partial underfill in the combined invention of White and Yan et al. as taught by Morganelli et al. to allow a space for volatile compounds to escape from the package during a reflow process (Morganelli et al., column1, lines 10-30, and column 8, lines 15-20).

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over White (US Patent No. 5,535,526) in view of Yan et al. (US Patent No. 6,841,888) and Morganelli et al. (US Patent No. 7,047,633) as applied to claim 5 above and further in view of Baba et al. (US Patent No. 6,582,993).

White, Yan et al. and Morganelli et al. do not expressly teach cleaning the organic board or substrate prior to depositing the underfill.

Baba et al. teaches cleaning the organic board or substrate prior to depositing the underfill to improve the wetness of the underfill receiving region.

Art Unit: 1793

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to cleaning the organic board or substrate prior to depositing the underfill in the combined invention of White, Yan et al. and Morganelli et al. as taught by Baba et al. to improve the wetness of the underfill receiving region.

7. Claims 15-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over White (US Patent No. 5,535,526) in view of Yan et al. (US Patent No. 6,841,888) and Morganelli et al. (US Patent No. 7,047,633) as applied to claim 5 above and further in view of Kumamoto et al. (US Patent No. 6,632,704).

White, Yan et al. and Morganelli et al. do not expressly teach the properties of the underfill material including density; particles size viscosity dynamic tensile modulus. Kumamoto et al., discloses the properties of a desirable epoxy underfill material applied in a surface-mount processing of an electronic devices for the purpose of relieving significant portions of thermal loads induced by coefficient of thermal expansion differences between a chip and a substrate (column 1, line 55- column 2, line 1). Kumamoto et al. also teaches an underfill material in its uncured state comprising a polymeric material having a filler material present in an amount ranging from about 80% by weight per solution said filler material having a particle size ranging from about 4 μ - 12 μ wherein said underfill material in its uncured state has a density of about 1.8 g/cc, a viscosity at 25.degree. C. greater than about 10,000 cP; wherein said underfill material in its cured state has a glass transition temperature ranging from about 145.degree. C; wherein said substrate comprises a ceramic substrate, said cured underfill material has

Art Unit: 1793

a CTE below Tg of about 14 ppm/degree. C and a CTE above the Tg of about 56 ppm/degree C (Kumamoto et al., table 1).

With respect to the tensile strength and the thixotropic index range, though not mentioned by Kumamoto et al., however, the numbers in table 1 of Kumamoto et al., closely match the corresponding numbers claimed by applicant, hence the tensile strength and the thixotropic index of Kumamoto et al. should necessarily be about the same as applicant's since said properties are intrinsic.

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to use in the combined invention of White, Yan et al. and Morganelli et al. the characteristic underfill material taught by Kumamoto et al. in order to increase the reliability and the fatigue resistance of the chip substrate interconnection (Kumamoto et al., column 1, lines 59-64).

Response to Arguments

8. The examiner acknowledges the applicants' amendment received by USPTO on October 02, 2007. Claims 11 and 12 have been cancelled, and therefore claims 1-10 and 13-22 are currently under consideration in the application.

9. Applicant's arguments with respect to claims 1-10 and 13-22 have been considered but are moot in view of the new ground(s) of rejection.

Art Unit: 1793

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Aboagye whose telephone number is 571-272-8165. The examiner can normally be reached on Mon - Fri 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jonathan Johnson can be reached on 571-272-1177. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



JONATHAN JOHNSON
PRIMARY EXAMINER



Michael Aboagye
Assistant Examiner
Art Unit 1725

10/12/2007

AM
AM